METHOD FOR PULSE TRAIN REDUCTION OF CLOCKING POWER WHEN SWITCHING BETWEEN FULL CLOCKING POWER AND NAP MODE

ABSTRACT

The present invention provides for reducing power across the entirety of a processor in a series of incremental steps. The clocking power requirements of a processor are evaluated through a power analysis and pre-programmed into a power train generator. A state machine control ramp logic comprising pre-programmed states resets a delay counter and issues state instructions to a pulse train generator. A pulse train generator outputs constant pulse trains and variable pulse trains that mask the original clocking power frequency. The pulse trains are distributed through a timed clock control distribution network to local clock buffers. The conditioned pulse trains step up or step down the clocking power, to the entirety of the processor, resulting in a smoothing of the clocking power switching. The smoothing of the clocking power reduces electrical spikes, surges and capacitance within the processor.